REMARKS

In the Office Action, claims 1, 4-6, 9, 11, 13-22 and 43-58 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Morioka et al. (U.S. Patent No. 5,274,434) taken with Morioka et al. (U.S. Patent No. 5,463,459) and Yamamoto et al. (U.S. Patent No. 5,623,340), and also with Levy (U.S. Patent No. 5,465,154).

Claims 1, 6, 9, 17, 43, 53, and 56 have been amended to more clearly describe the claimed invention. Claims 4 and 11 have been canceled. Claims 1, 5-6 and 9, 13-22, and 43-58 are now pending.

Independent claims 1, 6, 17, 43, 53, and 56 pertain to systems wherein a tool, such as a modular inspection system, a measurement tool, etc., is placed proximate to a window of a wafer handling chamber such that the tool is outside of a vacuum environment that is contained within the wafer handling chamber. The inventions of these claims are particularly advantageous over the prior art because the tool is configured to inspect a wafer that is in the wafer handling chamber, as opposed to a wafer that is in a processing chamber. In the opposing configuration, the required window quickly becomes obstructed by, for example, vapor of a chemical vapor deposition process. Also, the free-floating vapor or plasma can cause unwanted light refraction that causes inaccurate inspection results. Additionally, processing chambers are crowded with process tools and therefore present more physical obstructions that make inspection processes more difficult. Therefore, inspecting a wafer in a wafer handling chamber is more effective than inspecting a wafer that is within an actual process chamber.

Morioka et al. (U.S. Patent No. 5,274,434) discloses that an inspection system can be placed in a transfer system between processing apparatuses, however, it does not teach or suggest that the inspection system can be placed outside of the transfer system.

Levy (U.S. Patent No. 5,465,154) and Saisho et al. (U.S. Patent No. 5,414,506) disclose inspection systems that operate through a window to inspect wafers that are within a semiconductor fabrication processing chamber. Levy and Saisho et al. are specifically focused to monitor wafers during fabrication processes. *See* the Field of Invention section for both patent references. This means that the inspection systems in these disclosures are positioned about process chambers, not wafer handling chambers. Therefore, it is submitted that Levy and Saisho et al. do not teach or suggest placing an inspection system proximate a window of a wafer handling chamber.

It is also respectfully submitted that none of the references of Morioka et al. (U.S. Patent No. 5,274,434), Morioka et al. (U.S. Patent No. 5,463,459), and Levy (U.S. Patent No.

5,465,154) teach or suggest a motivation to combine any of their respective disclosures to result in the inventions of claims 1, 6, 17, 43, 53, and 56. Specifically, none of the cited references teach or suggest an inspection tool that is proximate to a window of a wafer handling chamber such that the tool is outside of a vacuum environment.

Therefore, it is respectfully submitted that independent claims 1, 6, 17, 43, 53, and 56 are patentably distinct from the cited references of Morioka et al. (U.S. Patent No. 5,274,434) taken with Morioka et al. (U.S. Patent No. 5,463,459) and Yamamoto et al. (U.S. Patent No. 5,623,340), and also with Levy (U.S. Patent No. 5,465,154). It is also submitted that dependent claims 5, 18-22, 44-52, 54-55, and 57-58 are patentably distinct from the cited references for at least the same reasons as stated above. In light of the foregoing, it is requested that the rejection of claims 1, 6, 17, 43, 53, and 56, and 5, 18-22, 44-52, 54-55, and 57-58 under 35 U.S.C. § 103(a) be withdrawn.

Independent claim 9 has been amended to more clearly define the invention. It is respectfully submitted that Morioka et al., Morioka et al., Yamamoto et al., and Levy do not teach or suggest all of the elements of claim 9. It is also submitted that claims 13-16, which depend from claim 9, are also patentably distinct from the cited references for at least the same reasons. Thus, it is respectfully requested that the Examiner withdraw the rejection of claims 9, 13-16 under 35 U.S.C § 103(a).

SUMMARY

It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 50-0388 (Order No. KLA1P001C1). A duplicate copy of the transmittal sheet for this amendment is enclosed for this purpose.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Five Times Amended) An integrated circuit manufacturing system comprising:

(a) a plurality of interrelated integrated circuit manufacturing tools capable of operating in parallel on a plurality of semiconductor wafers, wherein the plurality of interrelated integrated circuit manufacturing tools comprise a cluster tool;

(b) a modular optical inspection system disposed proximate to a window of a **central wafer handling chamber that is connected to each** **[cooling stage of the plurality]** of **the** interrelated integrated circuit manufacturing tools, the modular optical inspection system being outside of a vacuum **[processing]** environment, the modular optical inspection system including

a plurality of modular inspection subsystems each configured to detect defects on a portion of a semiconductor wafer,

a mechanism for moving at least one of the semiconductor wafer and the plurality of modular inspection subsystems with respect to one another, and

a master processor configured to process data delivered from at least some of the modular inspection subsystems, wherein a first one of the plurality of modular inspection subsystems includes a local processor configured to process data collected by the first modular inspection subsystem; and

(c) a handling tool for moving the semiconductor wafers among the plurality of manufacturing tools and the inspection system.

6. (Four Times Amended) In an integrated circuit manufacturing system including a plurality of interrelated integrated circuit manufacturing tools capable of operating in parallel on a plurality of semiconductor wafers, a method of inspecting a semiconductor comprising:

transferring the semiconductor wafer from one of the plurality of manufacturing tools to a modular optical inspection system that is disposed above a window of a **central wafer handling chamber that is connected to each** **[cooling tool]** of the plurality of interrelated integrated circuit manufacturing tools, the modular optical inspection system being outside of a vacuum **[processing]** environment, the modular optical inspection system including a plurality of modular inspection subsystems each configured to detect defects on a portion of the semiconductor wafer, wherein the plurality of manufacturing tools comprise a cluster tool; and

moving at least one of the semiconductor wafer and the plurality of modular inspection subsystems with respect to one another such that each of the modular inspection subsystems

inspects, in a single pass across the semiconductor wafer, an associated region of the semiconductor wafer.

9. (Twice Amended) A modular optical inspection system for inspecting a surface, the inspection system comprising:

a plurality of modular inspection subsystems each configured to detect defects on a portion of the surface;

a mechanism for moving at least one of the surface and the plurality of modular inspection subsystems with respect to one another, wherein at least one of the plurality of modular inspection subsystems includes

(i) a two-dimensional sensor configured to receive light from the surface; and

(ii) a controller configured to control the relative speeds at which

data is read from the sensor and

the modular inspection subsystem and the surface are moved with respect to one another

such that the surface is imaged in a time-delay integration mode,

wherein all of the plurality of modular inspection subsystems include separate sensors and separate controllers, and wherein each controller causes one row of pixel data to be read from a respective two-dimensional sensor each time the at least one inspection subsystem moves by one pixel length with respect to the surface**, and wherein each of the modular inspection subsystems has a field of view spanning a fraction of the width of the surface**.

17. (Four Times Amended) A modular optical inspection system for inspecting a surface, the inspection system comprising:

a plurality of modular inspection subsystems each configured to detect defects on a portion of the surface;

a mechanism for moving at least one of the surface and the plurality of modular inspection subsystems with respect to one another; and

a master processor configured to process data delivered from at least some of the modular inspection subsystems,

wherein a first one of the plurality of modular inspection subsystems includes a local processor configured to process data collected by the first modular inspection subsystem, also wherein the modular optical inspection system is disposed above a window of a **central wafer handling chamber that is connected to each [cooling tool]** of a plurality of integrated circuit

manufacturing tools, the modular optical inspection system being outside of a vacuum **[processing]** environment, the plurality of integrated circuit manufacturing tools being a cluster tool.

43. (Once Amended) An apparatus for processing semiconductor wafers comprising:

a wafer handling module containing an internal cavity, the wafer handling module having a port;

a process tool connected to the wafer handling module through the port;

a process sensor located proximate to the port **and proximate to a window of the wafer handling module wherein the process sensor is located outside of a vacuum environment that is contained within the internal cavity of the wafer handling module**; and

a handling mechanism located within the wafer handling module configured to transport a semiconductor wafer between the wafer handling module and the process tool.

53. (Once Amended) An apparatus for processing semiconductor wafers comprising:

a wafer handling module containing an internal cavity, the wafer handling module having a plurality of ports;

a plurality of process tools, each of the process tools connected to the wafer handling module through a respective one of the ports;

an inspection tool configured to detect defects on a semiconductor wafer, the inspection tool located proximate to a first one of the plurality of ports;

a thickness measurement tool configured to measure the thickness of materials deposited onto the semiconductor wafer, the thickness measurement tool located proximate to a second one of the plurality of ports**, wherein both the inspection tool and the thickness measurement tool are also located proximate to a window of the wafer handling module and are outside of a vacuum environment that is contained within the internal cavity of the wafer handling module**; and

a handling mechanism located within the wafer handling module configured to transport the semiconductor wafer between the wafer handling module and each of the process tools.

56. (Once Amended) An apparatus for processing semiconductor wafers comprising:

a wafer handling module containing an internal cavity, the wafer handling module having a plurality of ports;

a plurality of process tools, each of the process tools connected to the wafer handling

module through a respective one of the ports;

a detector configured to measure critical dimensions of integrated circuits upon a semiconductor wafer, the detector located proximate to a first one of the plurality of ports;

a thickness measurement tool configured to measure the thickness of materials deposited onto the semiconductor wafer, the thickness measurement tool located proximate to a second one of the plurality of ports**, wherein both the detector and the thickness measurement tool are also located proximate to a window of the wafer handling module and are outside of a vacuum environment that is contained within the internal cavity of the wafer handling module**; and

a handling mechanism located within the wafer handling module configured to transport the semiconductor wafer between the wafer handling module and each of the process tools.